



6 / 4 formal  
drawings  
e. Willis  
8-21-02  
219.40780X00

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: B. CHANDRAN ET AL.

Serial No.: 10/023,723

Filing Date: December 21, 2001

For: SEMICONDUCTOR PACKAGE WITH LOW RESISTANCE  
PACKAGE-TO-DIE INTERCONNECT SCHEME FOR  
REDUCED DIE STRESSES

**LETTER SUBMITTING FORMAL DRAWINGS**

Assistant Commissioner for Patents  
Washington, D.C. 20231

February 6, 2002

Sir:

Submitted herewith are three (3) sheets of formal drawings illustrating  
Figs. 1-10 in connection with the above-identified application.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Ronald J. Shore  
Registration No. 28,577

RJS:alw  
(703) 312-6600